CLAIMS:

1. A scheduling apparatus capable of providing an interface between a memory and at least a first and second device, the scheduling apparatus comprising:

a memory request arbiter capable of controlling access to the memory by different devices having different priorities; and

at least one counter coupled to the memory request arbiter, wherein the at least one counter is associated with at least the first device of the at least two devices, and wherein the at least one counter enforces a time-period that precludes access by the first device to the memory.

2. The scheduling apparatus according to claim 1, wherein the scheduling apparatus provides scheduling of tasks, at least one of the tasks not inherently having a pre-determined periodic behavior.

3. The scheduling apparatus according to claim 1, wherein the scheduling apparatus is capable of arbitrating access to memory by at least one device that is sensitive to latency and does not have a determinable periodic behavior.

4. The scheduling apparatus according to claim 1, wherein the first device associated with the counter is a CPU.

5. The scheduling apparatus according to claim 4, wherein the CPU is a high-priority device.

6. The scheduling apparatus according to claim 1, wherein

the first device associated with the counter is a graphics device.

7. The scheduling apparatus according to claim 1, wherein the at least two devices comprise a CPU and a graphics device.

8. The scheduling apparatus according to claim 7, wherein the scheduling apparatus is realized on an integrated circuit chip, and wherein the graphics device is incorporated onto the integrated circuit chip.

9. The scheduling apparatus according to claim 7, wherein the graphics device comprises at least one selected from a group consisting of a graphics accelerator and a display engine.

10. The scheduling apparatus according to claim 6, wherein the graphics device comprises one selected from a group consisting of a graphics accelerator and a display engine.

11. The scheduling apparatus according to claim 6, wherein the graphics device is a high priority device.

12. The scheduling apparatus according to claim 1, wherein the memory request arbiter is configured to arbitrate access to the memory by at least one device that does not have a determinable periodic behavior.

13. The scheduling apparatus according to claim 12, wherein the memory request arbiter is further configured to

arbitrate access to the memory by at least one other device that has a determinable periodic behavior.

14. The scheduling apparatus according to claim 1, wherein the at least one counter is programmable.

15. The scheduling apparatus according to claim 1, wherein the at least one counter produces the time-period in response to a memory access request by the first device.

16. The scheduling apparatus according to claim 1, wherein the at least one counter produces the time-period in response to a memory access by the second device.

17. The scheduling apparatus according to claim 1, wherein the at least one counter produces the time-period in response to a memory request by the second device.

18. The scheduling apparatus according to claim 1, wherein the at least one counter produces the time-period in response to completing a memory access by the second device.

19. The scheduling apparatus according to claim 1, wherein the at least one counter produces the time-period in response to completing a memory request by the second device.

20. The scheduling apparatus according to claim 1, wherein the scheduling apparatus is further capable of controlling access to the memory by a window controller.

21. The scheduling apparatus according to claim 1, further comprising a server coupled between the memory arbiter and at least two devices, wherein the server is capable of scheduling tasks from the at least two devices.

22. The scheduling apparatus according to claim 21, wherein the scheduling of tasks is round robin.

23. The scheduling apparatus according to claim 21, wherein the tasks comprise low priority tasks.

24. The scheduling apparatus according to claim 21, wherein the tasks comprise tasks from a high priority device whose associated counter is precluding it from getting a high priority service.

25. A scheduling apparatus capable of providing an interface between a memory and at least two devices, the scheduling apparatus comprising:

a memory request arbiter capable of controlling access to the memory for different devices having different priorities; and

at least one counter coupled to the memory request arbiter, wherein the at least one counter is associated with at least a first device of the at least two devices, and the counter being associated with time-periods, wherein during such time-periods the arbiter prevents the first device from accessing the memory,

wherein the scheduling apparatus provides scheduling of tasks, at least one of the tasks not inherently having a pre-determined periodic behavior, and

wherein the scheduling apparatus is capable of arbitrating access to at least one device that is sensitive to latency.

26. A scheduling apparatus capable of providing an interface between a memory and at least two devices, the scheduling apparatus comprising:

a memory request arbiter capable of controlling access to the memory for different devices having different priorities; and

at least one counter coupled to the memory request arbiter, wherein the at least one counter is associated with at least a first device of the at least two devices, and the counter being associated with time-periods, wherein during such time-periods the arbiter prevents higher priority devices from accessing the memory,

wherein the scheduling apparatus provides scheduling of tasks, at least one of the tasks not inherently having a pre-determined periodic behavior, and

wherein the scheduling apparatus is capable of arbitrating access to at least one device that is sensitive to latency.

27. A scheduling apparatus capable of providing an interface between a memory and at least two devices, the scheduling apparatus comprising:

a memory request arbiter capable of controlling access to the memory for different devices having different priorities;

and

at least one counter associated with the memory request arbiter, the counter using time-periods during which at least one of the devices will not have high priority access to the memory.

28. The scheduling apparatus of claim 27, wherein during the time periods at least one of the devices will not have high priority access to the memory, but will have low priority access.

29. The scheduling apparatus of claim 27 configured to provide scheduling of tasks, at least one of the tasks not inherently having a pre-determined periodic behavior.

30. The scheduling apparatus of claim 27 configured to arbitrate access by at least one device that is sensitive to latency.

31. A scheduling apparatus capable of providing an interface between a memory and at least two devices, the scheduling apparatus comprising:

a memory request arbiter capable of controlling memory requests for different devices having different priorities; and

at least one counter associated with the memory request arbiter, the counter using time-periods during which at least one of the devices will not make high priority requests to the memory.

32. The scheduling apparatus of claim 31, wherein during the time periods at least one of the devices will not make high priority requests to the memory, but will be able to make low priority requests.

33. The scheduling apparatus of claim 31 configured to provide scheduling of requests, at least one of the requests not inherently having a pre-determined periodic behavior.

34. The scheduling apparatus of claim 31 configured to arbitrate requests by at least one device that is sensitive to latency.